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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,497	10/26/2001	Er-Xuan Ping	MTI-31041-A	8624

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EXAMINER

LE, THAO X

ART UNIT PAPER NUMBER

2814

DATE MAILED: 11/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

10/046,497

Applicant(s)

PING ET AL.

Examin r

Thao X Le

Art Unit

2814

-- The MAILING DATE of this communication appears n the cover sheet with the correspondenc address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 October 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 101-193 is/are pending in the application.
- 4a) Of the above claim(s) 117-122, 136 and 161-164 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 101-116, 123-135, 137-160 and 165-190 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 11/2 & 6.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species b claims 101-116, 123-135, 137-160, 165-193 in Paper No. 7 is acknowledged. The traversal is on the ground(s) that the invention, which the Examiner has grouped separately, is not "independent and distinct". This is not found persuasive because the buried drain region would be distinct and independent from raised drain region.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 123-128 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 123 lines 5-6, recited 'each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material'. The 'overlying layer of an insulative materials' was not described in the specification. Claims 124-128 are rejected at least for being depended on rejected independent claim 123.

Art Unit: 2814

3. Claims 143-148 and 167-169 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 143 lines 2-3, recited 'each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material'. The 'overlying layer of an insulative materials' was not described in the specification. Claims 144-148 and 167-169 are rejected at least for being depended on rejected independent claim 143.

4. Claims 149-155, 170-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 149 lines 2-3, recited 'each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material'. The 'overlying layer of an insulative materials' was not described in the specification. Claims 150-155, 170-172 are rejected at least for being depended on rejected independent claim 149.

5. Claims 176-178, 179-181, 186-189, and 190-193 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claims 149, 179 lines 2-3, recited 'each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material'. The 'overlying layer of an insulative materials' was not described in the

Art Unit: 2814

specification. Claims 176-178 are rejected at least for being depended on rejected independent claim 176.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 123-128, 143-148, 167-169, 149-155, 170-172, 176-178, 179-181, 186-189, and 190-193 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Recited 'each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material' in the base claims 123, 143, 149, 167, 170, 176, 179, 186, and 190 is unclear, because such overlying layer of insulative material would prevent the electrical conductivity.

7. For the purpose of the examination, the examiner assumes that ~~each~~ epitaxial layer ~~STACK~~ comprises a top surface and sidewalls.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 101-109, 110-116, 123-128, 149-155, 179, are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of JP 2001068671 to Ri in view of US 5902125 to Wu.

Regarding to claim 101, 179, Ri discloses a transistor in a semiconductor device fig. 3A-3D comprising, source/drain (S/D) diffusion regions 27 formed on the semiconductive region of a substrate 20, the transistor gate 23 formed on the semiconductive region between the S/D diffusion regions 27, the transistor gate extending in a vertical orientation from the substrate 20, the transistor gate having insulated sidewall 26.

But Ri reference does not expressly disclose a transistor gate 23 comprises at least two overlying layers of epitaxial silicon and an uppermost layer having an insulated top surface.

However, Wu reference discloses the transistor gate 8 comprises at least tow overlying layers of silicon, column 4 line 3, uppermost layer having an insulated top surface 26, fig. 8. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to combine the multiple silicon layers teaching of Wu with Ri's device, because it would have prevented the penetration of the dopant through as taught by Wu, column 4 line 17-18.

Furthermore, the process limitations “epitaxially grown silicon” in claim 101 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding to claims 102-106, 111-114, 124-128, Ri discloses the transistor wherein the S/D diffusion regions 27 are elevated and extend in a vertical orientation from the substrate adjacent to the transistor gate 23, fig. 3D, wherein each of the S/D diffusion regions comprises at least two overlying layers 27a and 27b of epitaxially grown silicon, each epitaxial layer having insulated sidewall 26, fig. 3D, wherein each S/D diffusion layer 27a/27b comprises a conductivity enhancing dopant, page 15 line second paragraph, wherein each S/D diffusion layer 27a/27b comprises a facet top surface 28, fig. 3c, wherein at least one of the epitaxial layer of the S/D diffusion regions comprises a gradient of dopant, page 15 line 14-15.

Regarding to claim 107, 115, Ri does not expressly disclose the transistor wherein each S/D diffusion layer 27a/27b layer about 50 nm – 200nm

But Ri discloses the transistor wherein each S/D diffusion layer 27a/27b layer about 25 nm – 100nm, page 14 line 13 and page 15 line 12. Accordingly, it would have been obvious to use (teaching of second reference) in the range as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding to claim 108-109, Ri discloses the dielectric isolation 21 region is a shallow trench isolation region comprising an oxide, page 12 line 14.

Art Unit: 2814

Regarding to claims 110, 123, Ri discloses a transistor in a semiconductor device fig. 3A-3D comprising: the transistor gate 23 formed on the semiconductive region of a substrate 20, and elevated source/drain (S/D) diffusion regions 27 formed on the semiconductive region adjacent to the transistor gate and extending in a vertical plane from the substrate 20 and comprising at least two overlying layer of epitaxially grown silicon, 27a/27b.

But Ri does not expressly disclose each S/D diffusion regions covered by a layer of insulative material. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to form a insulative material on the S/D diffusion regions, because such insulation layer provides the protection or isolation of gate and S/D regions for further connection are well know in the art

Regarding to claim 116, as discussed in claims 101 and 110, both Ri and Wu combination discloses all the limitations in claim 116.

Regarding to claim 149-155, as discussed in the above claims, Ri and Wu combination discloses all the limitation in claims 149-155.

9. Claims 129-130, 132-135, 140-142, 143, 173, 182-185, 187-189, 190-193 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 2001068671 to Ri in view of US 5,970,351 to Takeuchi

Regarding to claims 129, 173, 143, Ri discloses the semiconductor structure in fig. 3D, comprising: at least two overlying layers 27a and 27b of epitaxial grow silicon, each epitaxial layer having insulated sidewalls 26, the structure disposed on a substrate 20 in a vertical orientation, the structure being a component of a transistor.

But Ri does not expressly disclose an uppermost epitaxial layer having an insulated top surface.

However, Takeuchi discloses a semiconductor structure in fig. 11c with an epitaxial layer 7A having an insulated top surface insulated 6B'. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the epitaxial layer having insulated surface the teaching of Takeuchi with the epitaxial layer 27a of Ri, because it insulated layer would provided a protection as n-channel or p-channel being created as taught by Takeuchi, column 11 lines 48-67 and column 12 lines 1-2.

Regarding to claim 130, Ri discloses the semiconductor structure wherein each epitaxial layer comprises a to surface defining a facet 28.

Regarding to claims 132-135, Ri discloses the semiconductor structure wherein each epitaxial layer has a thickness of up to about 200 nm, 50-200 nm, 70-100 nm and at least about 10 nm to 30 nm, page 14 second paragraph and page 15 first and second paragraph, and begin a component of a transistor.

Regarding to claim 140-142, Ri discloses the semiconductor structure 257 fig. 3D is being a source and drain region, wherein the uppermost and each epitaxial layer comprises a conductivity enhancing dopant, page 16 second paragraph.

Regarding to claims 156 and 158-160, Ri discloses the structure 257 fig. 3D is being a component of a transistor and is being a source and drain region, and wherein at least one of the epitaxial layer of the source and drain diffusion regions comprise a conductivity enhancing

dopant, and further comprises a concentration gradient of conductivity enhancing dopant, page 15 and 16 second paragraph.

Regarding to claims 165-166, 175 Ri discloses the semiconductor structure wherein the transistor is isolated by at least one shallow trench isolation region 21 formed in the substrate adjacent thereto, and the structure being a S/D diffusion region 27a/27b.

Regarding to claims 182-185, 187-189, 190-193, Ri discloses the semiconductor device comprising a semiconductor structure in fig. 3D, comprising: at least two overlying layers 27a and 27b of epitaxial grow silicon, each epitaxial layer having insulated sidewalls 26, the structure disposed on a substrate 20 in a vertical orientation, wherein the structure comprising a transistor and transistor gate 23, and S/D diffusion region 27a/27b.

But Ri does not expressly disclose an uppermost epitaxial layer having an insulated top surface.

However, Takeuchi discloses a semiconductor structure in fig. 11c with an epitaxial layer 7A having an insulated top surface insulated 6B'. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the epitaxial layer having insulated surface the teaching of Takeuchi with the epitaxial layer 27a of Ri, because it insulated layer would provided a protection as n-channel or p-channel being created as taught by Takeuchi, column 11 lines 48-67 and column 12 lines 1-2.

10. Claim 131 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP 2001068671 to Ri in view of US 5963822 to Saihara et al.

Regarding to claim 131, Ri does not expressly disclose the facet has a (100) plane orientation.

However, a silicon substrate would have having a plane orientation of (100) or (111) as discloses by Saihara. At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to form an epitaxial layer 27a of Ri having a plane orientation of (100), because such orientations are conventional and common for monocrystalline silicon substrate.

11. Claims 129, 137-139 and 156-157, and 173-174 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5902125 to Wu.

Regarding to claims 129, 173, Wu discloses the semiconductor structure in fig. 8, comprising: at least two overlying layers of silicon, each layer having insulated sidewalls 14, and an uppermost epitaxial layer having an insulated top surface 26, the structure disposed on a substrate 2 in a vertical orientation.

At the time the invention was made; it would have been obvious to one of ordinary skill in the art to replace the stacked-amorphous silicon (SAS) layer 8 teaching of Wu with epitaxial grown silicon layers, because such epitaxial grown silicon would have been considered a mere substitution of art-recognized equivalent values. Furthermore, the process limitations "epitaxially grown silicon" in claim 129 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding to claims 137-139, 156-157, 174, Wu discloses the structure being disposed adjacent to S/D region 22, being a component of a transistor, being a transistor gate 8, wherein the transistor gate is isolated within the substrate by at least one dielectric isolation region 4 disposed in the substrate adjacent thereto.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
November 22, 2002


PHAT X. CAO
PRIMARY EXAMINER